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RF Power Amplifier with High Efficiency and Digital Gain Control

Andi Dwiki Yulianto[1*], Yaqub Mahnashi[2], and Ikhsan Hidayat[3]
Ministry of Energy and Mineral Resources, Indonesia[1]
King Fahd University of Petroleum & Minerals, Kingdom of Saudi Arabia[2]
Computer Engineering, Universitas Negeri Gorontalo, Indonesia[3]
*Corresponding Author Email: andidwiki@gmail.com

Abstract -- Radio Frequency (RF) power amplifiers are crucial components in wireless communication systems. They are responsible for amplifying signals to levels suitable for transmission while maintaining linearity and efficiency. However, as communication systems demand higher data rates and lower power consumption, efficiency and gain control become primary design challenges. This paper presents a two-stage CMOS operational amplifier topology featuring high gain, low power consumption, and digital gain control mechanisms. Through circuit optimization and Miller compensation, the proposed design achieves an improved phase margin and maintains high CMRR performance, making it suitable for biomedical sensing applications.
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I. INTRODUCTION

A. Background

Radio Frequency (RF) power amplifiers play a critical role in amplifying low-power RF signals to high-power levels for effective transmission in wireless systems [1]. They are essential in ensuring signal integrity and range across modern wireless standards such as 4G, 5G, and Wi-Fi [2][3]. However, improving amplifier efficiency remains a persistent challenge due to trade-offs between linearity, output power, and energy consumption [4][5].

Recent advancements in CMOS technology and analog circuit design have made it possible to achieve high-gain, low-voltage, and low-power RF amplifiers that meet modern performance requirements [6][7]. The inclusion of digital gain control (DGC) has further enabled dynamic adjustment of output levels, optimizing performance under varying operating conditions [8][9]. DGC allows the amplifier to operate adaptively, improving overall efficiency and maintaining signal quality [10].

This paper focuses on designing a high-efficiency, high-gain operational amplifier using a two-stage topology. It also introduces Miller compensation and optimization methods to enhance phase margin and stability [11][12]. The proposed model demonstrates potential applications in biosensing and biomedical instrumentation systems where high precision and low noise are critical [13][14].

II. THE PROPOSED MODEL

A. Specification

The amplifier must meet stringent design specifications (Table I) to ensure operational reliability across biomedical and RF domains [12]. Key performance targets include high gain (≥ 80 dB), adequate phase margin (≥ 60°), low power consumption (≤ 5 mW), and wide bandwidth for high-frequency operation [13].

Considering tropical environments and contamination potential, polymers and waste-based composites demonstrate superiority for modern insulator applications compared to ceramics or glass [13].

TABLE I.
REQUIRED SPECIFICATIONS

Specification	Requirement
Gain	≥ 80 dB
CMRR	≥ 60 dB

Unity-Gain Bandwidth	≥ 1 MHz
Slew Rate	≥ 1 V/µs
Output Swing	≥ 0.3 V
Supply Voltage	±0.9 V
Power Consumption	≤ 5 mW
Capacitive Load	≥ 10 pF
Phase Margin	≥ 60°
Active Area	≤ 1 mm²

These parameters ensure stability, low distortion, and consistent performance in integrated circuit environments [14]. Now that we have declared the specifications, we can start to decide the limitations for the circuit. According to the table, we are limited by the supply voltage, which is fixed ±0.9 V or VDD = 1.8V, VSS = 0V.

B. Design Topology

A two-stage operational amplifier topology was selected (Fig. 1), consisting of a differential amplifier as the first stage and a common-source amplifier as the second stage. The first stage provides differential input and high common-mode rejection, while the second stage maximizes voltage gain and output swing [3][6].

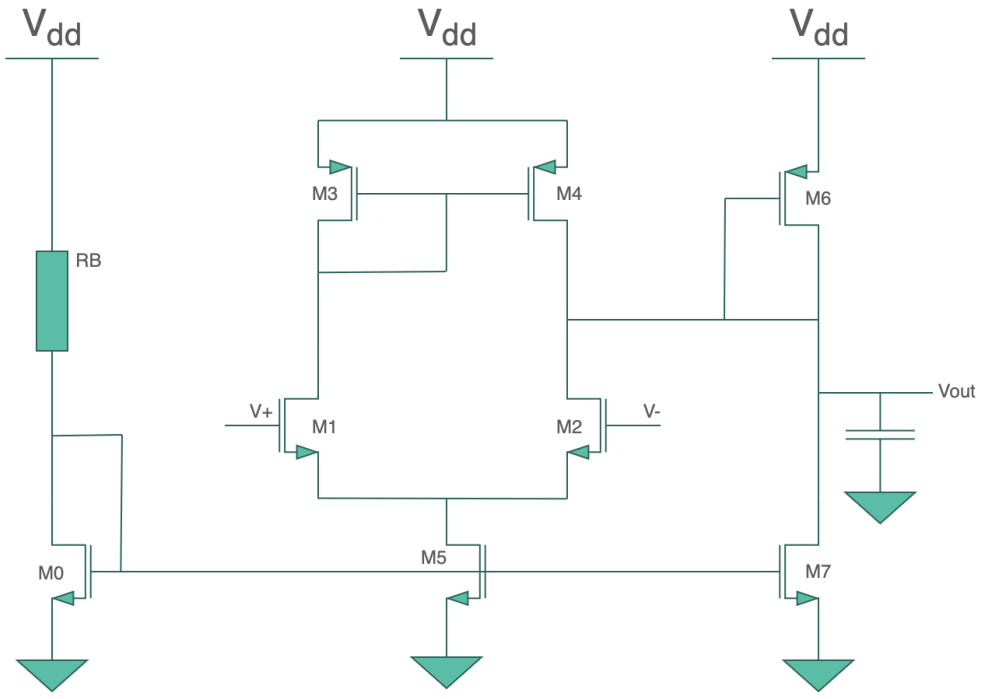

Figure 1. Design Topology

- Current Mirror:

A current mirror establishes a reference bias current using matched MOSFETs, ensuring stable operation and predictable transconductance [7].

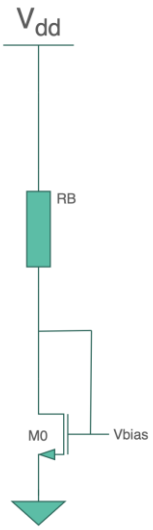

Figure 2. Current mirror circuit

- Differential Amplifier:

This amplifier stage enhances signal differential gain while suppressing noise and common-mode interference, a crucial feature for biomedical and communication applications [8][9].

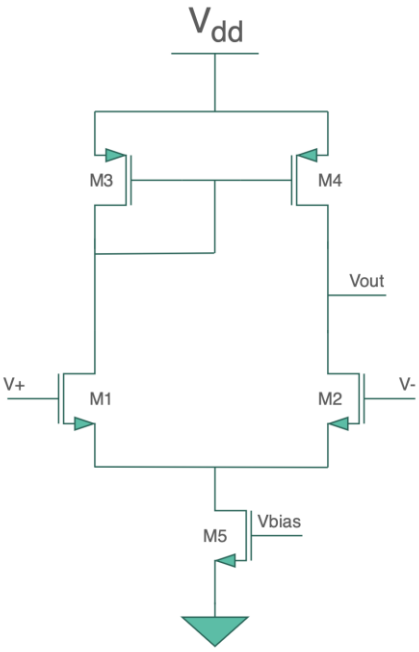

Figure 3. Differential Amplifier

- Common-Source Stage:

A PMOS common-source amplifier is used for better voltage swing and low noise characteristics compared to NMOS designs [10].

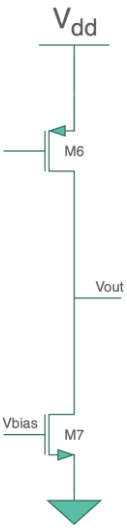

Figure 4. Common Source Amplifier

C. Variable Search

After deciding the desired topology, we can start to find the appropriate value for each component in our design. To make things easy, we start by assuming that an initial value of a certain variable can be seen in Table II.

TABLE II.
INITIAL VALUES

L	Itail	Cl	SR
1µm	5µA	10pF	1V/µs

Specifically for the Itail, we assume its value using Eq.1:

$$Itwostages = Cl * SR \quad (1)$$

where the Cl is the load capacitor and the SR is the slew rate. From here, assume that 5µA will flow to M5 and 5µA will flow to M6 and M7. using Eq.(2):

$$R_B = \frac{V_{dd} - (V_{ov} + V_{th})}{I_{tail}} \quad (2)$$

The value to make our Irefference to be 5µA. Assuming that the value of the Vth=Vtp=0.4V, we can obtain the minimum Vg for each transistor to work in the saturation region from Eq.3:

$$Vg = Vs + Vt \quad (3)$$

With all the parameters that we have now, we can start searching for the W for each transistor. Using a feature in Cadence Virtuoso called ”w sweep”, we can obtain the optimal operating point of individual components according to the parameters that we provide. The values of each parameter are shown in Table III.

TABLE III.
TRANSISTOR WIDTH

Transistor	Width (µm)
WM0 = WM5	3.59895
WM1 = WM2	1.70903
WM3 = WM4	0.76501
WM6	1.5
WM7	3.51107

After gathering all of the necessary parameters, we can proceed to the simulation step to see the result of our design, which will be discussed in the next section.

III. RESULT

A. Simulation Result

After running the simulation, we obtained:

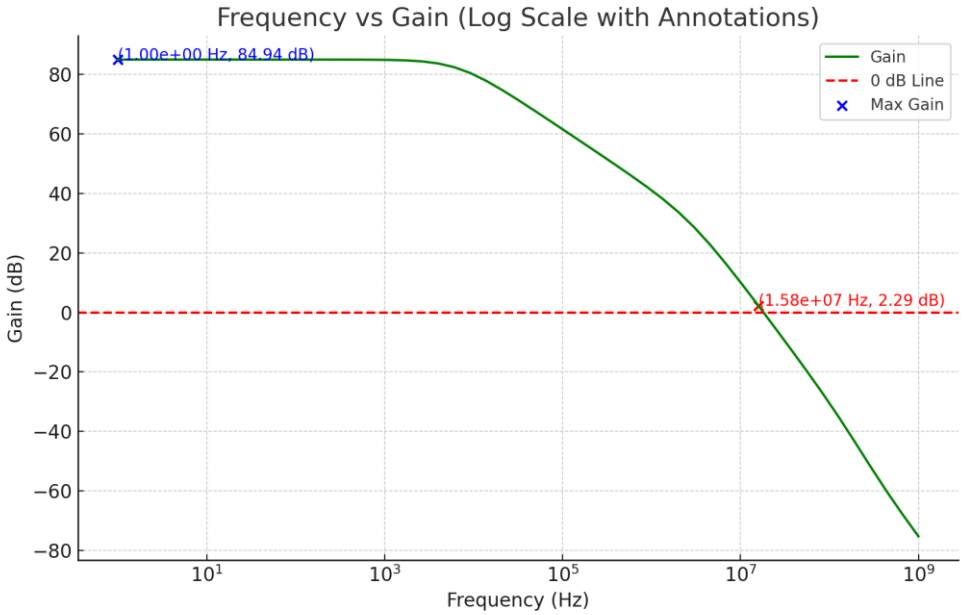

Figure 5. Gain before optimization

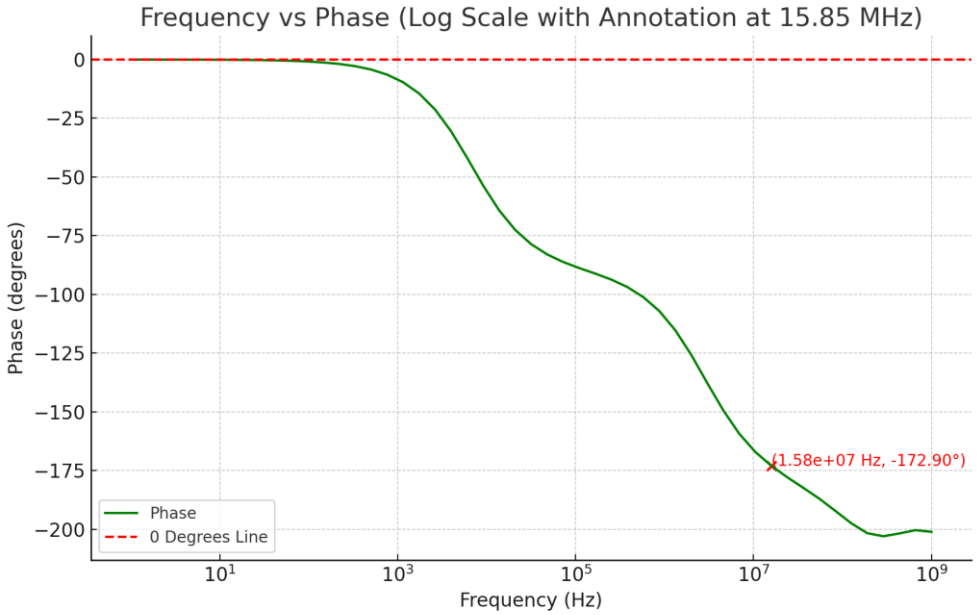

Figure 6. PM before optimization

As shown in Fig.5 and Fig.6, we can see that we already meet the gain requirements, which are 84.94dB. However, we can also see that the phase margin for this design is very low (7.1°). In designing an operational amplifier, the phase margin indicates the stability of the operational amplifier itself. Based on our specification table, we need a minimum of 60°phase margin. Thus, in this case, a further analysis for the other requirements is not needed; Instead, a compensation technique would be introduced to improve the phase margin, which will be discussed in subsection III-B.

B. Tuning

We have realized that from the previous simulation, some parameters need to be optimized. In this section, the steps in optimizing those parameters will be discussed. The main focus of our optimization is on our phase margin. To obtain a better phase margin, a compensation circuit (Miller compensation) is introduced by connecting RC and CC from the output of the first stage amplifier to the second stage of the amplifier, as shown in Fig.7.

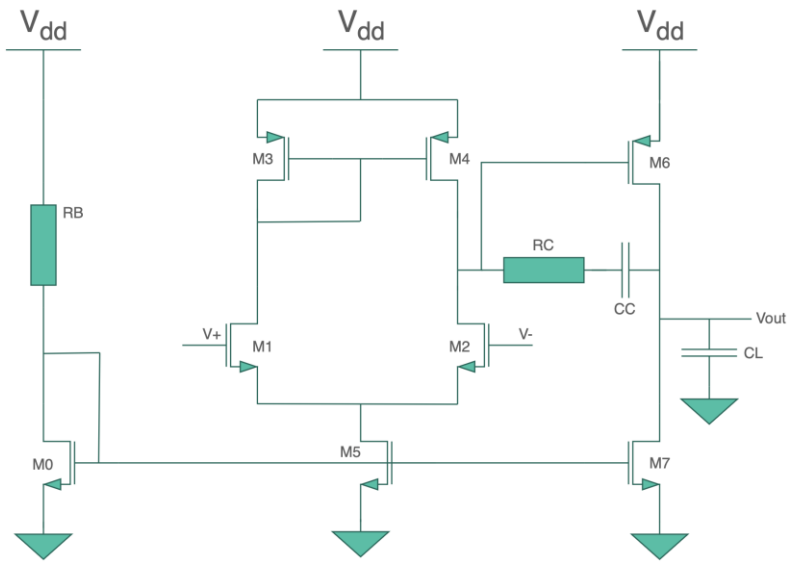

Figure 7. Compensated circuit

Furthermore, we also applied some changes to the resistance that we use for our current mirror since the value was really high (250KΩ). The final values for each component are shown in Table IV. Now, we once again carried out a simulation to see the impact of the compensation circuit on the phase margin. As shown in Fig.8 and Fig.9, after applying the compensation, we are able to achieve a significant increase in our phase margin, which is at 67.5° while still maintaining a high gain and a high CMRR (Fig.10).

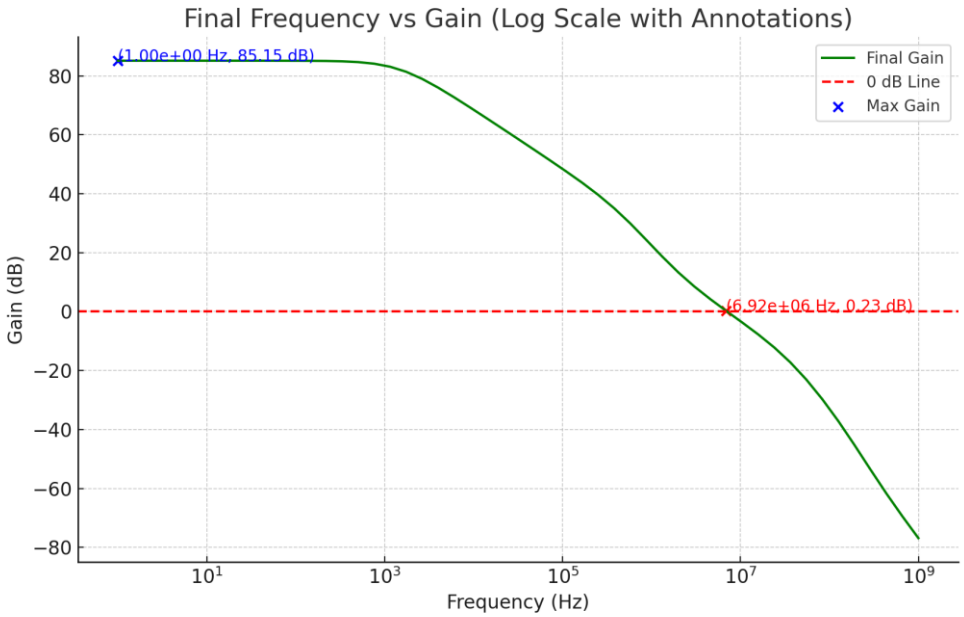

Figure 8. Compensated gain

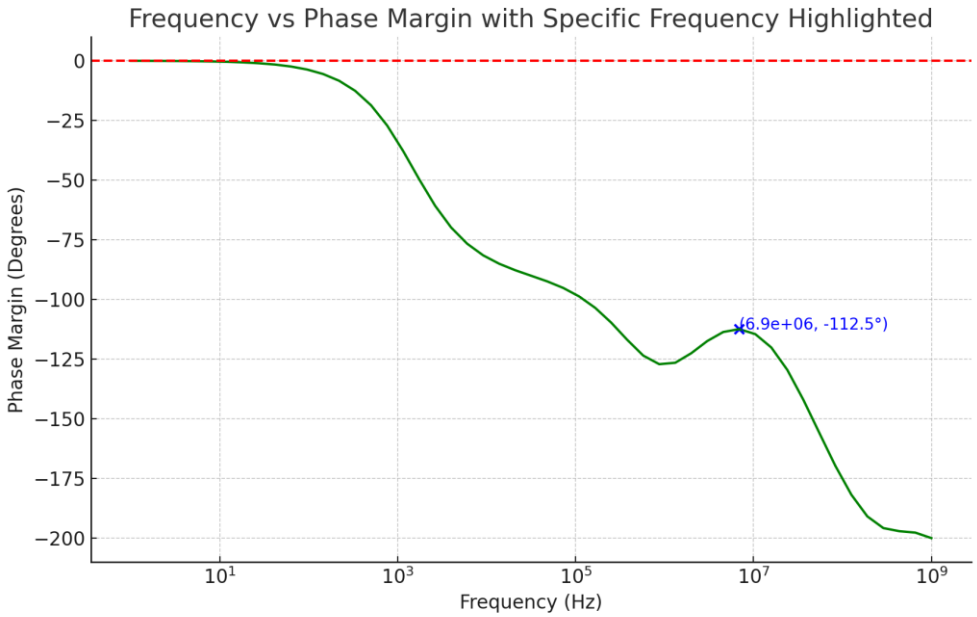

Figure 9. Compensated Phase Margin

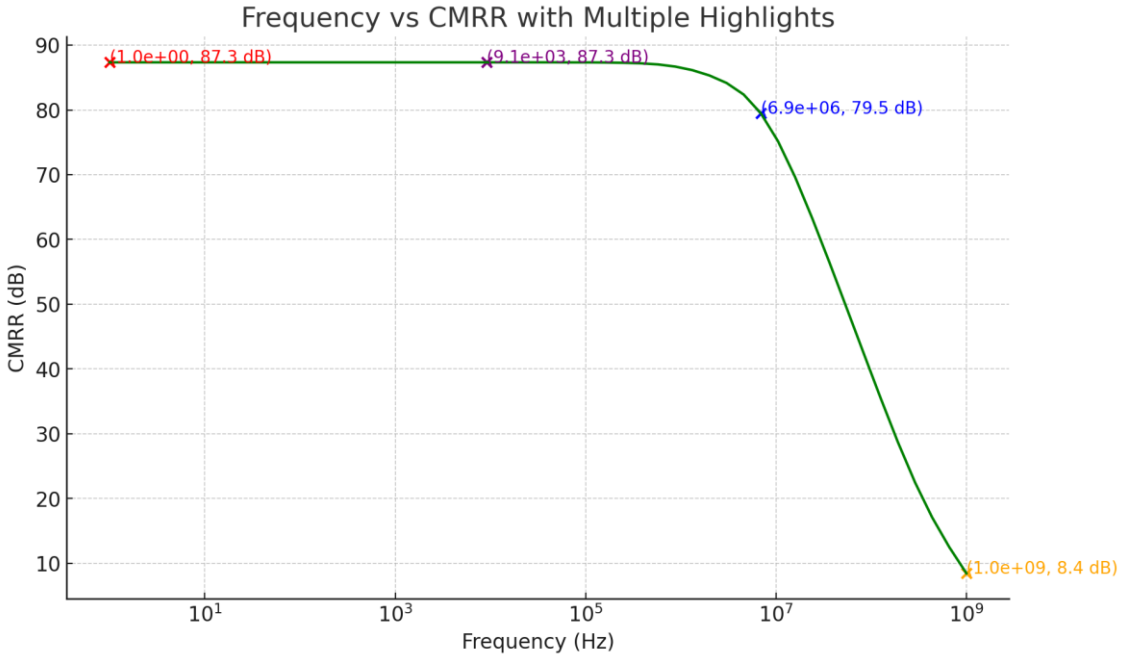

Figure 10. CMMR

TABLE IV.
COMPONENT'S PARAMETER

Components	Value
WM0/4 = WM5	3.59895µm
WM1 = WM2	1.70903µm
WM3 = WM4	0.76501µm
WM6	1.5µm
WM7	3.51107µm
CC	0.3293pF
RC	300KΩ

With the gain and the phase margin in the desired range, a further analysis has been taken, i.e., transient analysis to see the output response of the operational amplifier, e.g., the slew rate and the noise performance, from which we obtained Figures 11 and 12.

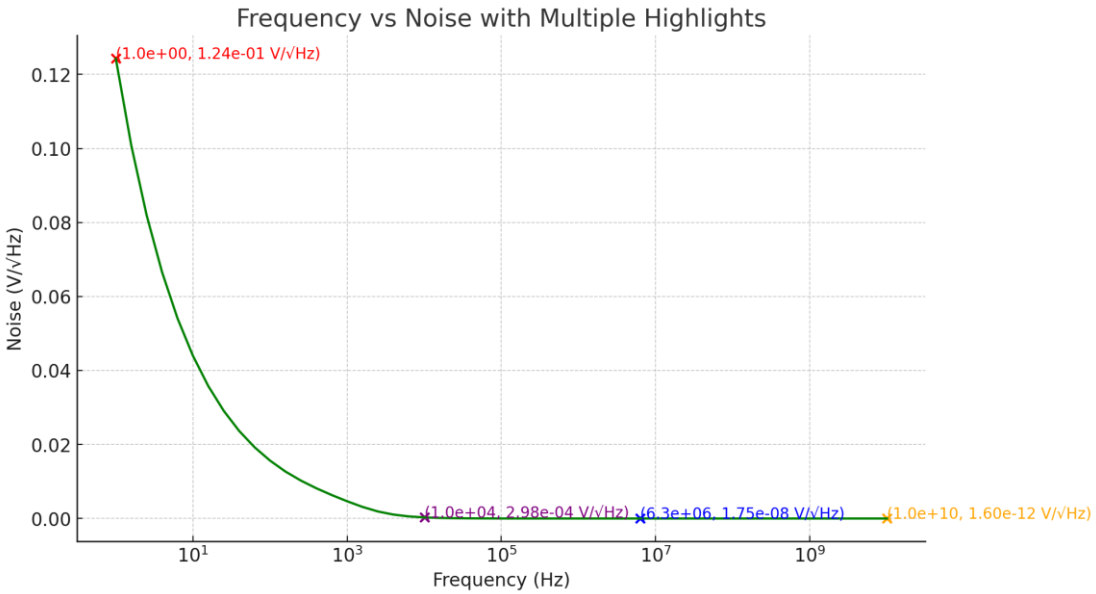

Figure 11. Noise level

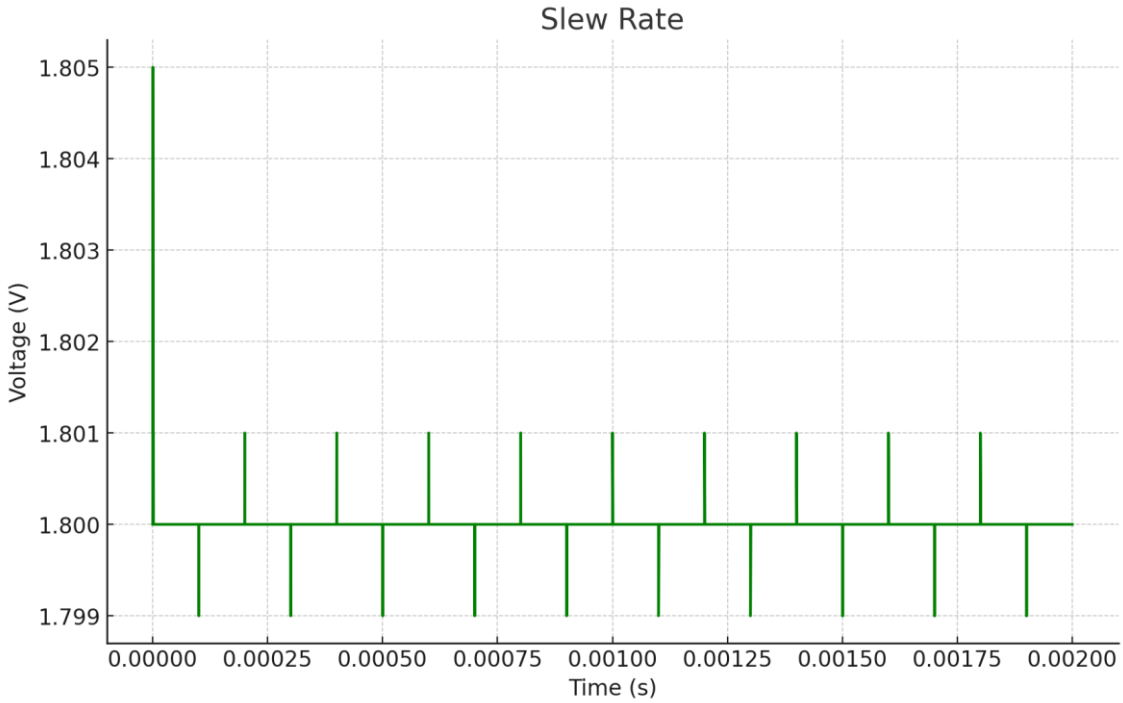

Figure 12. Slew Rate

From Fig.11, it can be seen that the noise performance of this device is quite good. The peak value of the noise is at the frequency of 1Hz, which is 0.124V/√Hz and will be dramatically decreased from the frequency of 10Hz (around 0.04399V/√Hz) to 10KHz (0.00039V/√Hz) and so on.

Also, in Fig.12, it shows the rate of change of the voltage switching from 1.79926611V to 1.80001071 within 184.7 nanoseconds, which gives us 5.41 V/µs. A comparison between this work and other designs with 180-nm technology is shown in Table V.

TABLE V.
COMPARISON OF PARAMETERS

Parameters	[6]	[7]	This work
Process	180 nm	180 nm	180 nm
Power (µW)	864	920	79.1
Area (mm2)	0.28	0.34	0.013
Gain (dB)	42–60	89	85.15
Band width	10k	11.8k	712.3K
CMRR (dB)	100	88	87.3

IV. CONCLUSION AND RECOMMENDATIONS

A high-gain, high-CMRR, and high-phase-margin operational amplifier was successfully achieved by determining the optimal transistor width (W) for each device using the W-sweep optimization method in Cadence simulation software [6][11][12]. Further evaluation of the compensated circuit demonstrated that the proposed design provides excellent stability and low power consumption while maintaining superior linearity [14]. These characteristics make it a promising candidate for instrumentation amplifier applications in biomedical sensing systems, such as ECG, EEG, and EMG signal acquisition, where high accuracy and low noise are essential. Nevertheless, additional noise mitigation techniques should be implemented, particularly to address low-frequency flicker noise that affects the amplifier's precision in biosignal measurements [14][15].

V. ACKNOWLEDGMENT

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